Model Predictive Control for Three-Phase Split-Source Inverter

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«Three-phase system», «MPC (Model predictive control) », «Modeling», «Converter circuits», «Converter control».

Abstract
This paper proposes a new topology of three-phase split-source inverter (SSI) with only one auxiliary power electronic switch inserted into the three-phase full-bridge inverter. Split-source inverter is a single stage topology, which combines the boosting stage with the DC/AC converter stage. The proposed three-phase SSI has fewer passive components than impedance source converters (like ZSI). Switching states of the conventional three-phase VSI can be used with the SSI to control the output voltage. An independent control for both DC link voltage and output AC voltage is achieved using model predictive control. The DC link voltage can be controlled via duty cycle obtained by a maximum power point tracker or by fixed duty cycle as used in this paper. Simulation results show that the proposed control achieves low THD of the AC output voltage (good performance) with both normal loading condition and sudden load change condition.

Introduction
Interest in single-stage buck/boost inverters has grown over the past few years due to the need to reduce the size as well as the cost of the overall system while increasing the efficiency of the power converter. The main application of single-stage boost inverters is in the PV-based systems. A conventional PV system consists of a DC/DC converter and a single/three phase inverter. The two-stage topology suffers from low efficiency and bulkiness, but it has simple control strategy. The single-stage buck/boost inverter topology, however, performs two advantageous functions: boosting the DC input voltage and ensuring that the output AC voltage is sinusoidal with low THD. Various circuit topologies of single-stage buck/boost topologies have been reported in the literature [1]-[3].

One of the single-stage boost inverter topologies is the split-source inverter (SSI) that has been reported in the literature [4]-[9]. SSI is a DC-AC boost inverter topology which requires a boosting inductor and a DC link capacitor, see Fig. 1. The single-phase SSI was first introduced in 2010 [4]. It consists of a single-phase H-bridge inverter with two common anode diodes connected in each leg and an inductor connected with a DC source and capacitor connected across the inverter legs, see Fig. 1.(*a*) [5]. The control strategy proposed is similar to that of the conventional single-phase H-bridge inverter, where, during the positive half cycle, switches Q_1 and Q_2 are turned ON/OFF and the other two switches are switched OFF. During the negative half cycle, Q_3 and Q_4 are turned ON/OFF while Q_1 and Q_2 are turned OFF. During either half cycle, the inductor is charged and discharged into the capacitor but with variable duty cycle leading to low frequency component at the DC side, which increases the conduction losses.

To overcome the problem of variable duty cycle and hence improve the overall system efficiency, an alternative SSI configuration has been introduced in [6]. The two diodes in that converter have been connected to a DC source with their common cathode configuration, see Fig. 1.(b). In that topology, the inductor was charged if one/both of the two upper switches were turned ON and discharged into the DC link capacitor when each of the upper switches were turned OFF. A modified SPWM technique has been used to achieve constant duty cycle, where the reference signals of each leg have been modified to be quasi-sinusoidal in a half cycle and constant in another half cycle. That guaranteed that one of the upper switches was turned ON/OFF constantly in each half cycle. However, both the SSIs in [5] and [6] have

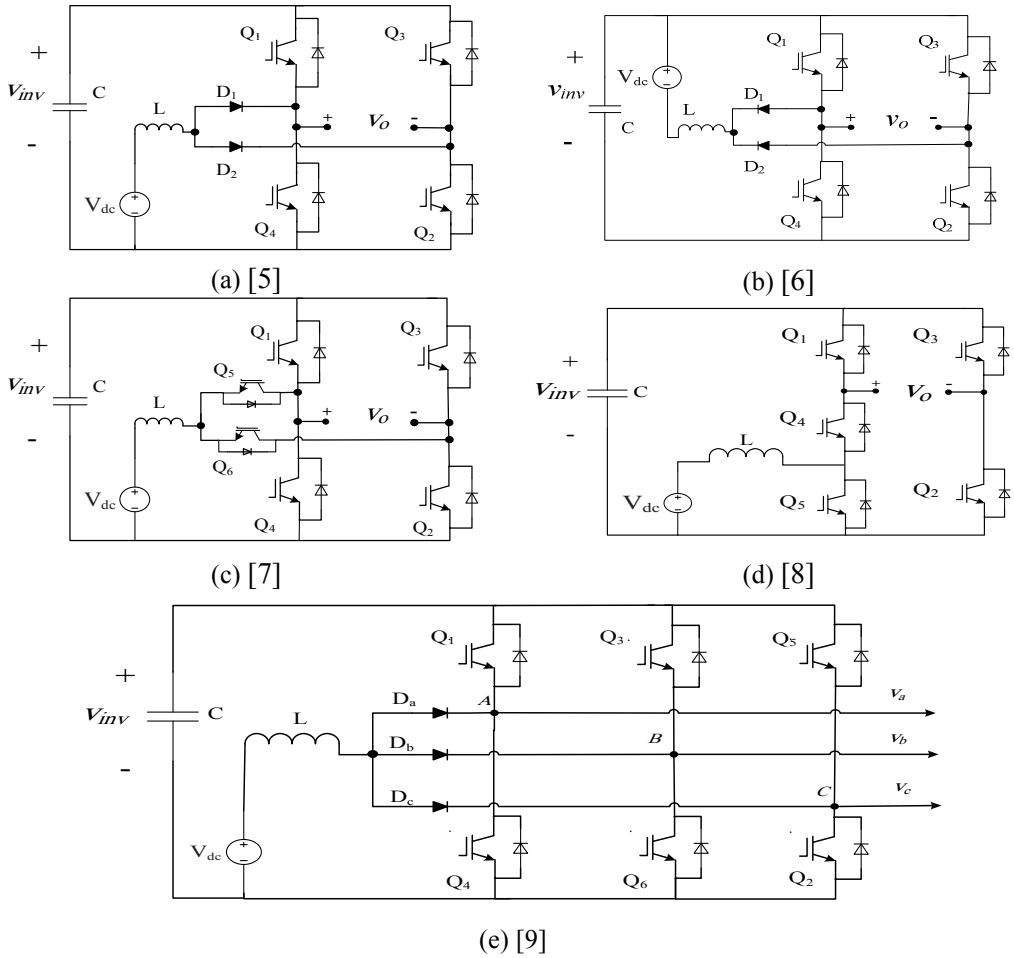

Fig. 1. Existing SSI topologies in the literature

been incapable of exchanging power with the DC source, i.e. no bidirectional power flow. Also, the power diodes suffered from high frequency commutation and hence losses.

To enable bidirectional power flow and reduce the high-frequency commutation of the diodes, the two input diodes have been replaced with two MOSFETs in [7], see Fig. 1.(c). A constant duty cycle was obtained by modifying the reference signals of each leg to be hybrid quasi-sinusoidal in half cycle and constant in the other half cycle. That converter topology had the same number of switches as that of the bidirectional converter and of the conventional single-phase H-bridge inverter but with a different switching arrangement.

To cut down on the number of switching devices, a simplified SSI (S^3I) has been introduced in [8], where only one auxiliary MOSFET was connected to one of the H-bridge legs, forming a one leg with three switches parallel to the two-switched leg of the inverter, see Fig. 1.(d). That topology reduced power switches, which enhanced power efficiency, increased voltage boosting gain, and reduced output filter requirements. Sinusoidal PWM has been used to control S^3I, where two sinusoidal waveforms with phase shift and constant waveforms were compared with carrier waveforms to control the two legs of the inverter and the auxiliary switch, respectively.

A three-phase SSI was introduced in [9], where three diodes were connected to the three legs of the inverter, see Fig. 1.(e). The inductor was energized if at least one of the bottom switches was turned ON. The inductor discharged into the capacitor when all the top switches were turned ON. The three-phase SSI was controlled by modified SVPWM (MSVPWM), where the reference signals were the same as those of the SVPWM with VSI, but the lower envelopes were constant. Hence, the duty cycle was fixed. However, that topology suffered from high-frequency commutations of the input diodes, which

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represented additional losses. Moreover, that converter was incapable of performing bidirectional power flow with the DC source.

This paper proposes a new topology of the three-phase SSI. The new three-phase SSI replaces three diodes in [9] with only one bidirectional switch, enabling bidirectional power flow (suitable for stand-alone PV systems with batteries) and reducing the system size. The proposed topology eliminates the high-frequency commutation of the input diodes, and improves efficiency due to low turn-ON resistance of the bidirectional switch [7], [8]. However, an additional gate driver is required for the bidirectional switch. The control of the proposed three phase SSI is achieved by finite control set model predictive control (FCS-MPC). FCS-MPC is used to control the traditional three-phase SSI as in [10]-[12]. FCS-MPC is suitable for the discrete nature of the power electronics converters and can deal with multivariable systems, constraints and nonlinearities[13], [14]. An independent control for both DC-link voltage and AC output voltage can easily be achieved.

The advantages of the proposed SSI topology are: 1) continuous input current, 2) continuous DC-link voltage, 3) less passive components, 4) lower stress on the switches at higher voltage gains, 5) maintaining the same switching state of VSI, and 6) enabling bidirectional power flow. On the other hand, the disadvantages are: 1) unbalanced current distribution among SSI switches, 2) higher current stress at high voltage gains, and 3) high voltage stress at low voltage gains.

Proposed Three-Phase SSI

The proposed three-phase SSI is shown in Fig. 2. The inductor L is charged if the auxiliary switch Q_7 is ON. While inductor L is charging, the SSI can operate with eight possible switching states of the three-phase VSI as shown in Fig. 3.(a). When the auxiliary switch Q_7 is turned OFF, the inductor L is discharging into a capacitor (C). At this moment, the three-phase SSI can operate with only four possible switching states as shown in Fig. 3.(b). The switch Q_7 can be controlled with a fixed duty cycle or by a duty cycle obtained from MPPT controller of a PV system to extract the maximum available power from the PV array and hence control the DC link voltage. The DC link voltage (v_{inv}) can be obtained from (1) [8] . The output AC voltage can be controlled by the PWM dictated by the model predictive control presented later in this article. An independent control for both DC-link capacitor voltage and output AC voltage can easily be provided. However, the three-phase SSI suffers from
unbalanced current sharing among the switches as shown in Table I. Yet, this is an inherent problem with all SSI topologies which can easily be resolved by paying attention to the sizing of the power electronic switches [8], [9].

$$v_{inv} = \frac{V_{dc}}{1-D} \tag{1}$$

Model Predictive Control

The proposed three-phase SSI is controlled by finite-control set model predictive control (FCS-MPC). FCS-MPC is suitable for power electronics converters since it uses the model of the system to predict the future behavior of the controlled variables for all possible voltage vectors of the converter and uses

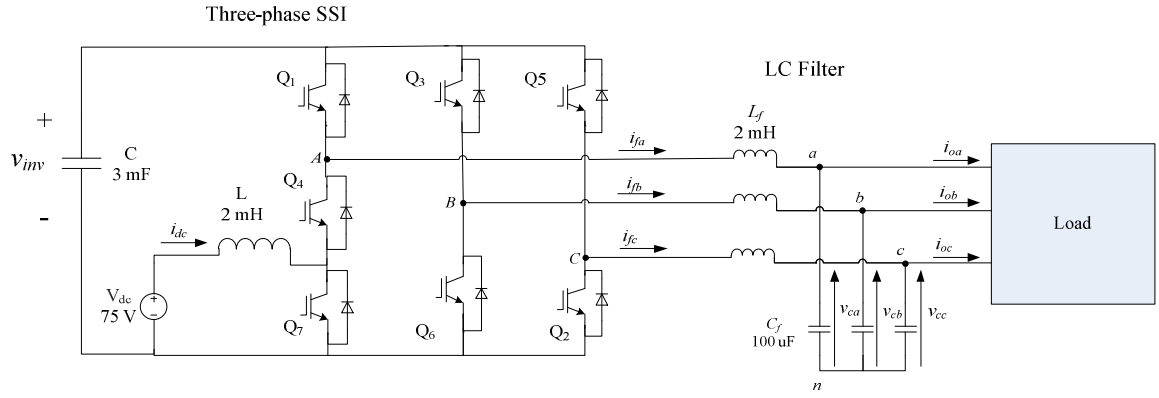

Fig. 2. The proposed three-phase SSI

Table I. Current and voltage stresses for the proposed SSI switches

Switch	Current stress	Voltage stress
Q_1: Q_6	$i_{f,\,ph}$	v_{inv}
Q_7	$i_{f,\,ph}+i_{dc}$	
Anti-parallel diode of Q_1	$i_{f,\,ph}+i_{dc}$	
Anti-parallel diode of Q_4	i_{dc}	
Anti-parallel diodes of Q_2, Q_3, Q_5, Q_6	$i_{f,\,ph}$	

the information to obtain optimal action by choosing the voltage vector that minimizes a cost function. The possible switching states and corresponding voltage vectors of the proposed three-phase SSI are shown in Fig. 3 and Fig. 4.

The Model of the System

The power circuit of a three-phase inverter with a second-order LC filter is shown in Fig. 2. The load voltage ($\boldsymbol{v}_c$), the inductor filter current ($\boldsymbol{i}_f$), and the load current ($\boldsymbol{i}_o$) are given by:

$$\boldsymbol{v}_c = \frac{2}{3}\left(v_{ca} + \boldsymbol{a}v_{cb} + \boldsymbol{a}^2 v_{cc}\right) \tag{2}$$

$$\boldsymbol{i}_f = \frac{2}{3}\left(i_{fa} + \boldsymbol{a}i_{fb} + \boldsymbol{a}^2 i_{fc}\right) \tag{3}$$

$$\boldsymbol{i}_o = \frac{2}{3}\left(i_{oa} + \boldsymbol{a}i_{ob} + \boldsymbol{a}^2 i_{oc}\right) \tag{4}$$

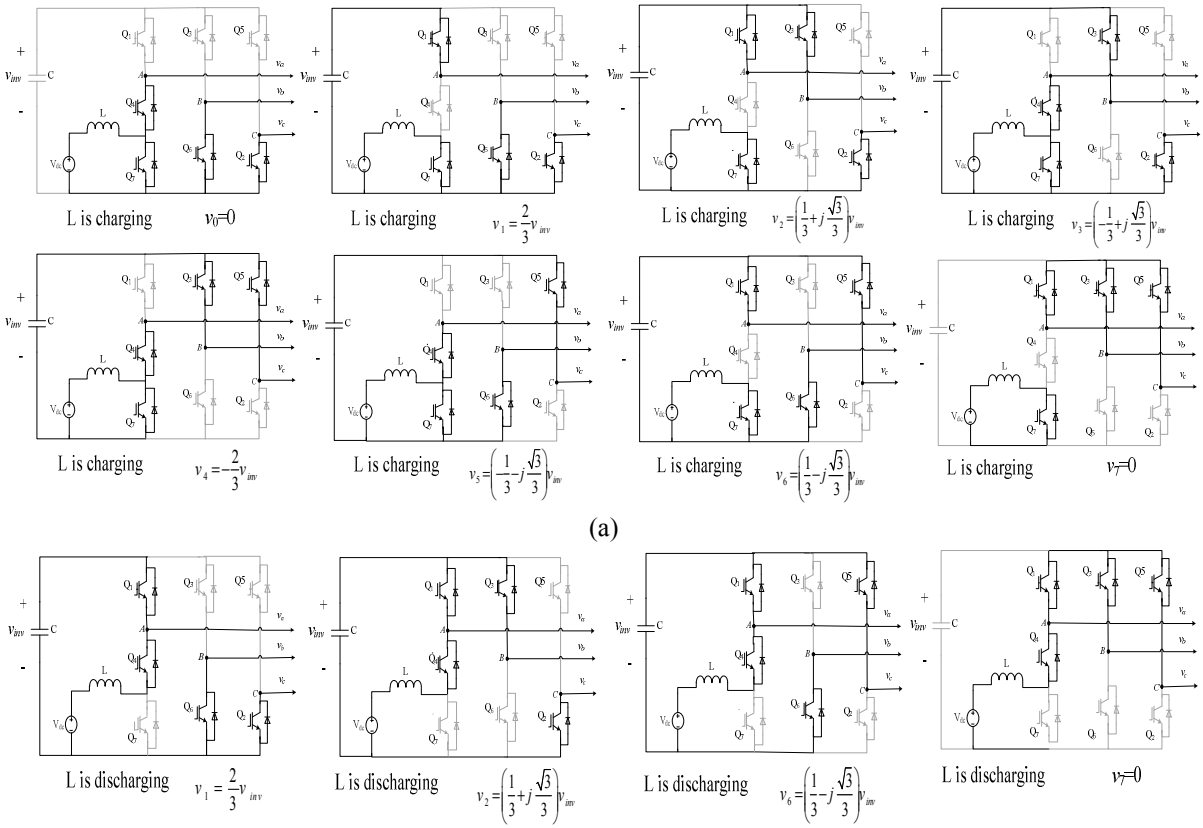

Fig. 3. Possible switching states of the proposed three-phase SSI at (a) charging L and (b) discharging L

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Where $\mathbf{a} = e^{j\frac{2\pi}{3}} = -\frac{1}{2} + j\frac{\sqrt{3}}{2}$ represents the 120° phase displacement between phases. The governing differential equations of the LC filter variables are:

$$L_f \frac{d\boldsymbol{i}_f}{dt} = \boldsymbol{v}_i - \boldsymbol{v}_c \tag{5}$$

$$C_f \frac{d\boldsymbol{v}_c}{dt} = \boldsymbol{i}_f - \boldsymbol{i}_o \tag{6}$$

Where, v_i, C_f and L_f are the SSI output voltage, filter capacitance and inductance, respectively. Equations (5) and (6) can be rewritten in a state-space variable format as:

$$\frac{d\boldsymbol{x}}{dt} = A\boldsymbol{x} + B\boldsymbol{v}_i + B_d \boldsymbol{i}_o \tag{7}$$

where,

$$\boldsymbol{x} = \begin{bmatrix} \boldsymbol{i}_f & \boldsymbol{v}_c \end{bmatrix}^T \tag{8}$$

$$A = \begin{bmatrix} 0 & \frac{-1}{L_f} \\ \frac{1}{C_f} & 0 \end{bmatrix} \quad B = \begin{bmatrix} \frac{1}{L_f} \\ 0 \end{bmatrix} \quad B_d = \begin{bmatrix} 0 \\ \frac{-1}{C_f} \end{bmatrix} \tag{9}$$

The system output equation is given by:

$$\boldsymbol{v}_c = \begin{bmatrix} 0 & 1 \end{bmatrix} \boldsymbol{x} \tag{10}$$

The discrete time model is obtained from (7) for a sampling time T_S and expressed as:

$$\boldsymbol{x}(k+1) = A_q \boldsymbol{x}(k) + B_q \boldsymbol{v}_i(k) + B_{dq} \boldsymbol{i}_o(k) \tag{11}$$

where

$$A_q = e^{AT_S} \quad B_q = \int_0^{T_s} e^{At} B dt \quad B_{dq} = \int_0^{T_s} e^{At} B_d dt \tag{12}$$

Model Predictive Control Strategy

FCS-MPC algorithm is shown in Fig. 5. The value of the output voltage ($\boldsymbol{v}_c$(k)), inductor filter current ($\boldsymbol{i}_f$(k)) and the load current ($\boldsymbol{i}_o$(k)) are measured at the current instance k. The condition of the switch Q_7 is observed. If Q_7 is ON, the SSI can operate with all possible voltage vectors as shown in Fig. 4. (a). If Q_7 is OFF, the SSI can only operate with four possible voltage vectors as shown in Fig. 4.(b). The output voltages, for every possible voltage vector, at next instance ($\boldsymbol{v}_c$(k+1)) can be predicted using (11). Then, the cost function (13) is used to select the voltage vector that gives the lowest error between reference and output voltages at next instance. Consequently, the corresponding switching state is applied in the next instance.

$$g = \left(v^*_{c\alpha} - v_{c\alpha}(k+1)\right)^2 + \left(v^*_{c\beta} - v_{c\beta}(k+1)\right)^2 \tag{13}$$

where, $v_{c\alpha}$ and $v_{c\beta}$ are the real and imaginary parts of the predicted output voltage vector $\boldsymbol{v}_c$(k+1). The control block diagram of the system is shown in Fig. 6. In the FCS-MPC, there is no need for a PWM modulator because the output of the controller itself is the switching signal.

Simulation Results

The proposed three-phase SSI with FCS-MPC is simulated using MATLAB/Simulink with the system parameters shown in Fig. 2. The load is linear with 0.9 power factor lag and 33 Ω impedance. The DC link voltage is controlled via the switch Q_7 by a fixed duty cycle (D) 0.83 and with a switching frequency of 20 kHz. The output AC voltage is controlled via the switches Q_1 - Q_6 using the FCS-MPC with 20 kHz switching frequency. The switching frequency of Q_7 must be equal to or less than the switching frequency of Q_1-Q_6. The DC link capacitor voltage (v_{inv}) is shown in Fig. 7. (*a*), and equal to 429.5 V. The boosting inductor current (i_{dc}) is shown in Fig. 7. (b) and equals nearly 23 A. The three-phase output voltage waveforms (v_{ca}, v_{cb}, v_{cc}) are shown in Fig. 8. The output voltages are sinusoidal with low THD of 1.64%. The peak value of the phase voltage at steady state is 197.2 V. Fig. 9.(a) shows the three-

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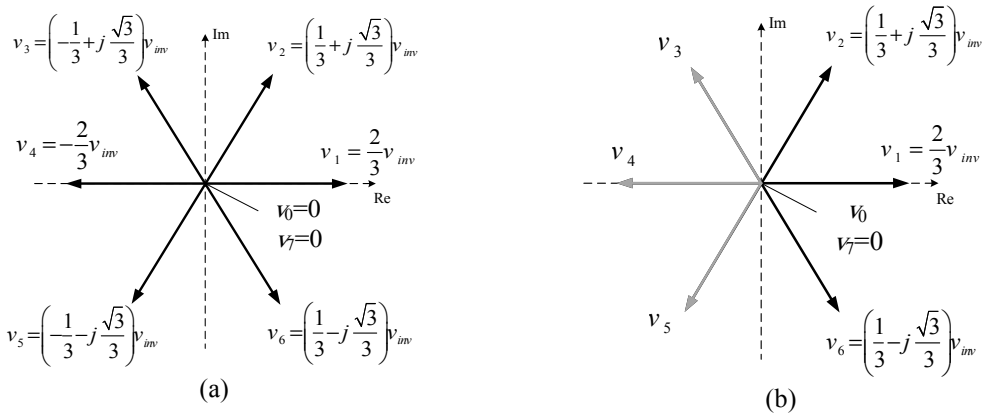


Fig. 4. Voltage vectors of the proposed three-phase SSI at (a) charging L, and (b) discharging L

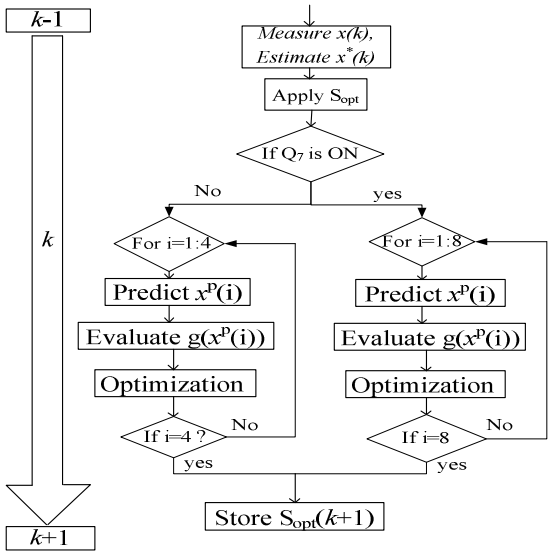


Fig. 5. FCS -MPC algorithm

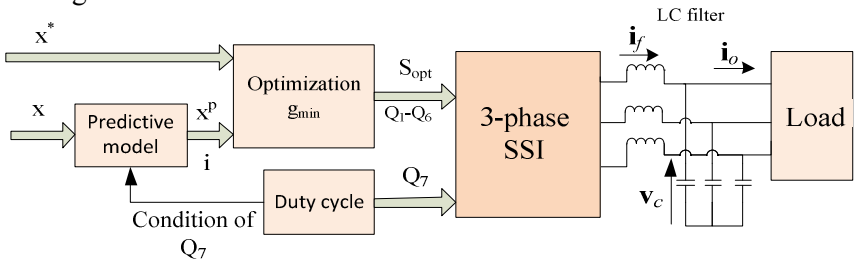
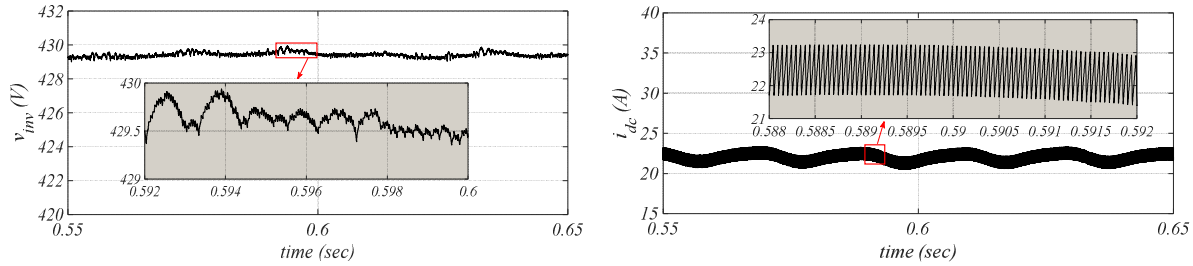


Fig. 6. System control block diagram

phase load currents (i_{oa}, i_{ob}, i_{oc}), which equals 4.2 A rms with 0.55% THD. Fig. 9.(b) shows the inductor filter currents (i_{fa}, i_{fb}, i_{fc}). The figure shows that the inductor filter current is rich of harmonics with a THD of 50.11%.

Q_1 current is shown in Fig. 10, where the positive part is the current in the IGBT and the negative part of the current is current passing through the anti-parallel diode. From the figure, the current of Q_1 in the IGBT is equal to the inductor filter current while the anti-parallel diode current is equal to the inductor filter current plus the boosting inductor current. Fig. 11 shows the current of the switch Q_4 which is equal to the inductor filter current while the anti-parallel diode is equal to the boosting inductor current. Fig. 12 shows that the currents of the IGBT and the anti-parallel diode of Q_3 combined are equal to the inductor filter current. The current of the switches Q_2, Q_5, and Q_6 are similar to that of Q_3. The current of the switch Q_7 is shown in Fig. 13 to be equal to the inductor filter current plus the boosting inductor current. The anti-parallel diode of Q_7 has no current because there is no bidirectional power flow between the load and the DC source. The switches currents are shown in Table I. From the above, the



(a) (b)

Fig. 7. (a) The DC-link capacitor voltage and, (b) the boosting inductor current

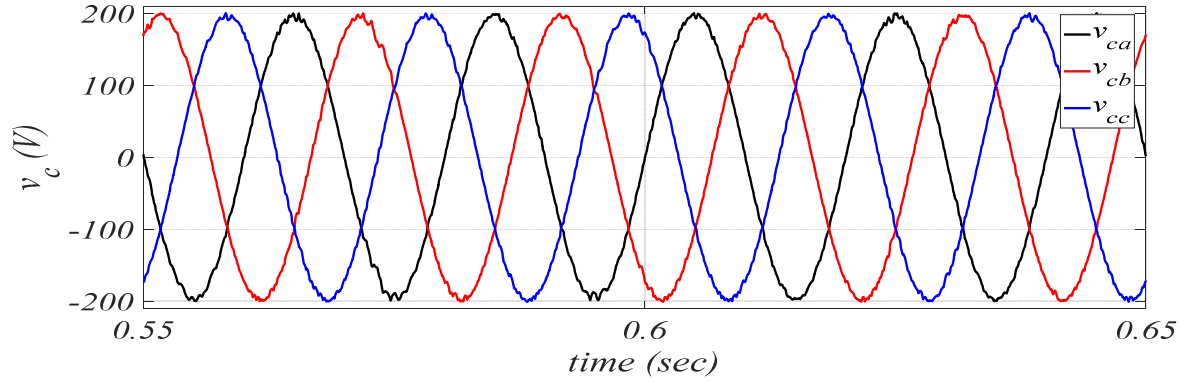
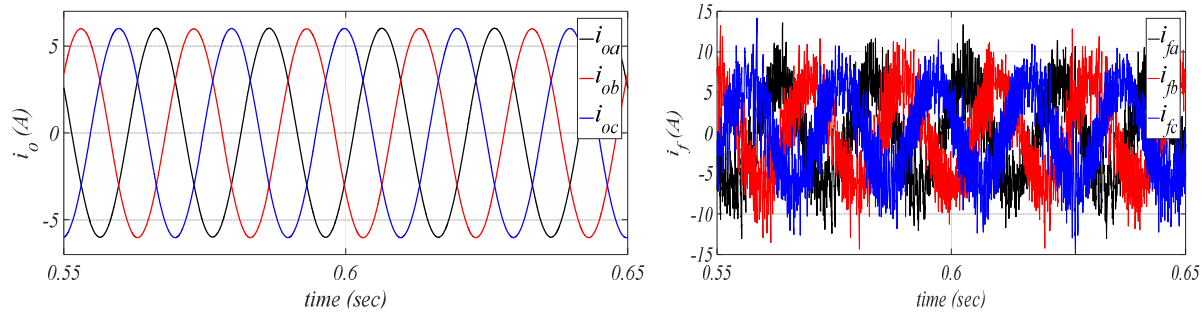


Fig. 8. Three-phase output voltage



(a) (b)

Fig. 9. Steady-state waveforms: (a) three-phase output current and, (b) three-phase inductor filter current

switches Q_1 and Q_7 should be selected to withstand the inductor filter current plus the inductor booting current. While the switch Q_4 should withstand the inductor boosting current, and the rest of the switches (Q_2, Q_3, Q_5 and Q_6) should withstand the inductor filter current.

The dynamic behaviour of the proposed inverter is investigated by applying sudden change in the load from 33 Ω at 0.9 p.f. lagging to a load of 21 Ω at 0.7 power factor lagging and is shown in Fig. 14. The load current waveforms (i_{oa}, i_{ob}, i_{oc}) before, during, and after load change are shown in Fig. 14.(a). The figure shows that the currents undergoes increase from 4.2 A to 6.7 A rms (almost 60% increase). The load currents take approximately 12.8 ms to reach its steady-state value. The three-phase output voltages (v_{ca}, v_{cb}, v_{cc}) waveforms are shown in Fig. 14.(b). The figure shows that there is a slight effect on the load voltage due to this sudden load change. The THD of the output voltages is 1.73%. The DC-link capacitor voltage (v_{inv}) is shown in Fig. 14.(c). The figure shows a slight decrease in the DC voltage from 429 V to steady-state value 426 V with an undershoot reaching 423 V (-1.3%). The boosting inductor current (i_{dc}) is shown in Fig. 14.(d), which has increased from 23 A to 28 A.

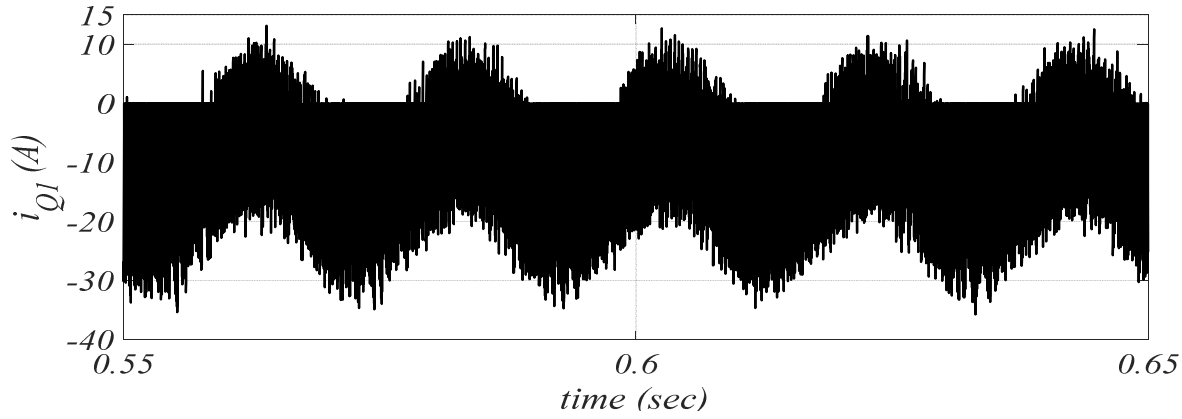


Fig. 10. The current of the switch (Q_1)

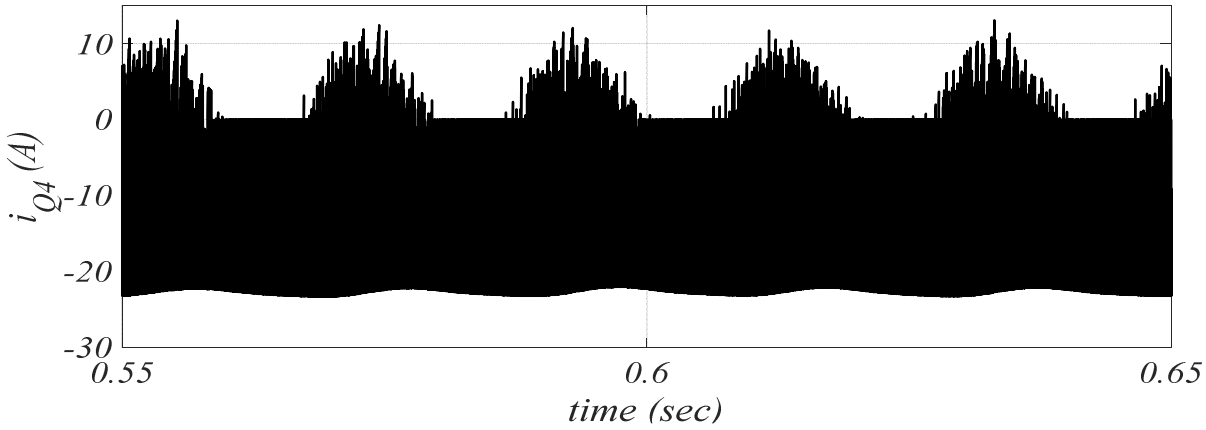
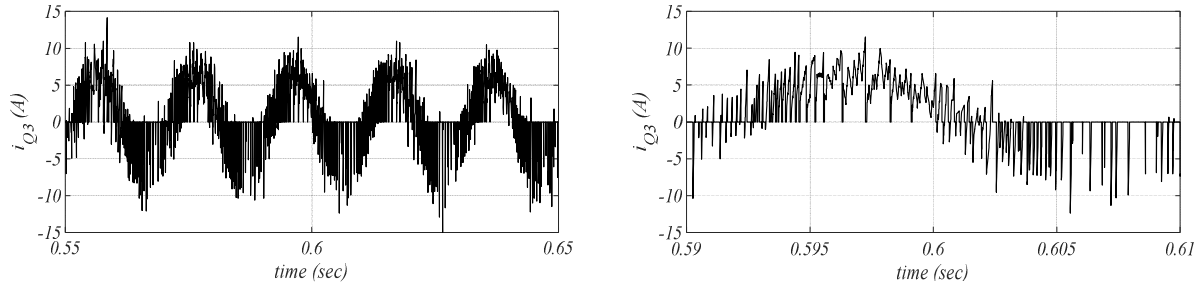


Fig. 11. The current of the switch (Q_4)



(a) (b)

Fig. 12. (a) The current of the switch (Q_3), (b) Zoom view for one cycle of the switch current

Another sudden change in the load from 21 Ω at 0.7 power factor lagging to 33 Ω at 0.9 power factor lagging. The load current waveforms (i_{oa}, i_{ob}, i_{oc}) are shown in Fig. 15.(a). The figure shows that load currents have decreased from 6.7 A to 4.2 A rms. The load currents take approximately 6.32 ms to reach its steady-state condition. The three-phase output voltages (v_{ca}, v_{cb}, v_{cc}) waveforms are shown in Fig. 15.(b). The figure shows that the load voltages are slightly affected due to the sudden load change. The THD of the output voltages is 1.97%. The DC-link capacitor voltage (v_{inv}) is shown in Fig. 15.(c). The figure shows a slight increase in the DC voltage from 426 V to a steady-stae value 429 V (approximately 0.7%) with overshoot reaches to 432 V. The boosting inductor current (i_{dc}) is shown in Fig. 15.(d). The figure shows that i_{dc} has decreased from 28 A to 23 A.

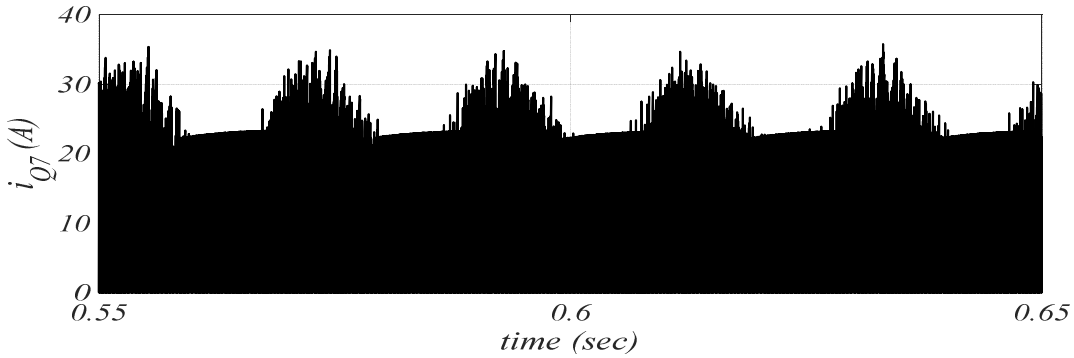


Fig. 13. The current of switch (Q_7)

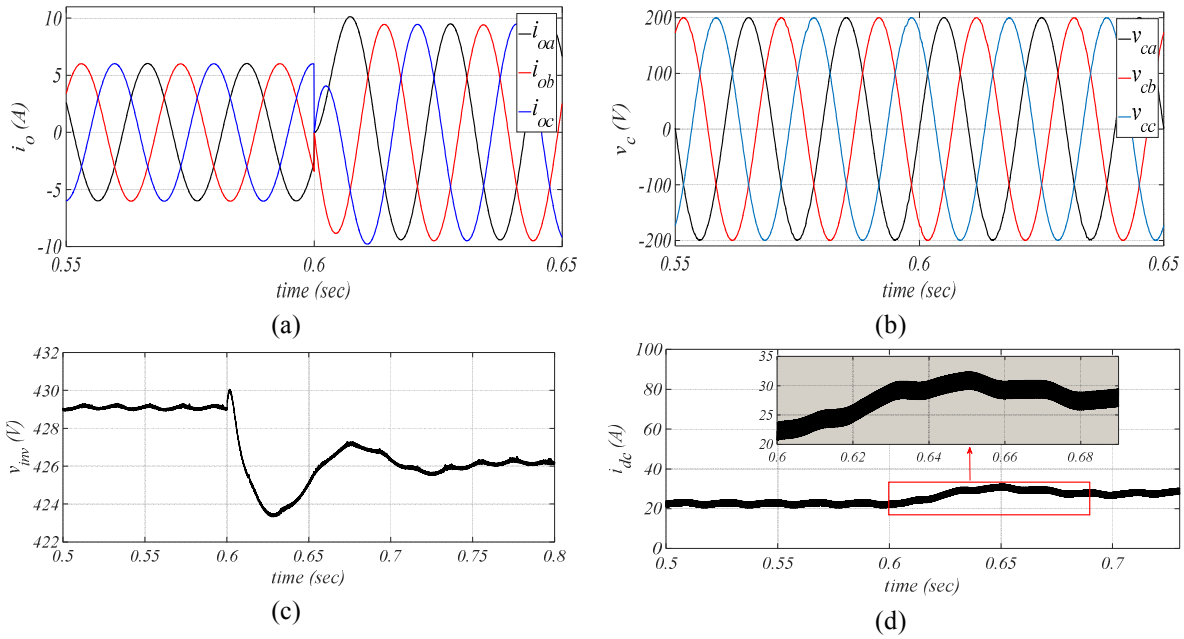


Fig. 14. Dynamic behavior of sudden increase in the load current of the proposed SSI: (a) three-phase output currents, (b) three-phase output voltages, (c) the DC-link capacitor voltage, and (d) the boosting inductor current

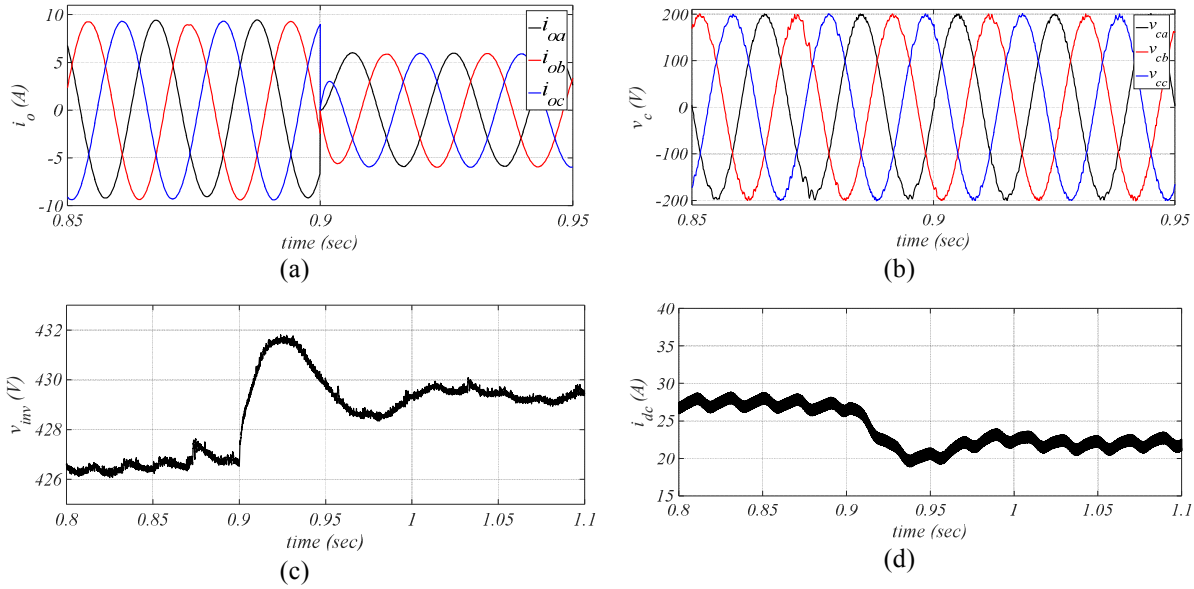


Fig. 15. Dynamic behavior of sudden decrease in the load current of the proposed SSI: (a) three-phase output current, (b) three-phase output voltage, (c) the DC-link capacitor voltage and, (d) the boosting inductor current

Conclusions

This paper proposed a new circuit topology for three-phase split-source inverter (SSI). The proposed SSI has advantage of bidirectional power flow capability, which is not provided in already existing three-phase SSI. This bidirectional power flow is specially needed for PV-based systems. The proposed SSI reduces the power semiconductor count of the three-phase SSI by replacing three diodes by only one bidirectional switch. This, in turn, reduces the high-frequency commutation of the input diodes and hence improves the overall efficiency. FCS- MPC is used as the control algorithm of the new topology. When the boosting inductor is charging, all switching states can be used, while only four switching states can be used at discharging of the boosting inductor. The proposed SSI is simulated with a linear load at both steady-state and dynamic phases. Under all operating conditions, the results show good load voltage regulation with low THD.

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